1. 1-17 (Cancelled).

18. (Currently Amended) A refractory metal liner, comprising:

a barrier comprising a passivating agent, said barrier impeding a subsequent reaction of at least a top half of said refractory metal liner with an adjacent conductive layer, an amount of said passivating agent in said carrier being less than an amount necessary to form a stoichiometric combination of said refractory metal liner and said passivating agent,

wherein said barrier is limited to a central portion of said refractory metal.

19. (Previously Presented) The refractory metal liner in claim 18, wherein impurities from said adjacent conductive layer are limited to said top half of said refractory metal liner.

20. (Previously Presented) The refractory metal liner in claim 19, wherein said barrier impedes impurities from diffusing from said adjacent conductive layer through said refractory metal.

21. (Original) The refractory metal liner in claim 20, wherein said impurities comprise silicon impurities.

22. (Original) The refractory metal liner in claim 19, wherein a second conductive layer is positioned over said refractory metal, said barrier impeding impurities from diffusing from said second conductive layer through said refractory metal.

23. (Original) The refractory metal liner in claim 22, wherein said impurities comprise fluorine impurities.

24. (Original) The refractory metal liner in claim 22, wherein:

said refractory metal comprises one of tungsten, titanum, molybdenum and nickel; and

said passivating agent comprises one or more of nitrogen and chlorine.

25. (Previously Presented) An electrical connection in an integrated circuit chip, said electrical connection comprising:

a first conductive layer;

a liner on said first conductive layer, said liner including a barrier, said barrier impeding first impurities from diffusing from said first conductive layer through said liner; and

a second conductive layer over said liner, wherein said barrier impedes second impurities from diffusing from said second conductive layer through said liner,

wherein said barrier is limited to a central portion of said liner, wherein said first impurities are positioned within the portion of said liner adjacent said first conductive layer and second impurities are positioned within the portion of said liner adjacent said second conductive layer.

26. (Currently Amended) ~~The electrical connection in claim 25,~~ An electrical connection in an integrated circuit chip, said electrical connection comprising:

a first conductive layer;

a liner on said first conductive layer, said liner including a barrier, said barrier impeding first impurities from diffusing from said first conductive layer through said liner; and

a second conductive layer over said liner, wherein said barrier impedes second impurities from diffusing from said second conductive layer through said liner,

wherein said barrier is limited to a central portion of said liner, wherein said first impurities are positioned within the portion of said liner adjacent said first conductive layer and second impurities are positioned within the portion of said liner adjacent said second conductive layer, and

wherein said barrier comprises a concentration of a passivating agent less than an amount necessary to form a stoichiometric combination with said liner.

27. (Previously Presented) The electrical connection in claim 26, wherein:
said liner comprises one of tungsten, titanum, molybdenum and nickel;
said passivating agent comprises one or more of nitrogen and chlorine; and
said second conductive layer comprises one of tungsten and copper.

28. (Currently Amended) The electrical connection in claim ~~25~~ 26, wherein said impurities comprise one or more of silicon impurities and fluorine impurities.

29. (Previously Presented) An integrated circuit chip comprising:
a first conductive layer;
a liner on said first conductive layer, said liner including a barrier, said barrier impeding first impurities from diffusing from said first conductive layer through said liner; and
a second conductive layer over said liner, wherein said barrier impedes second impurities from diffusing from said second conductive layer through said liner,
wherein said barrier is limited to a central portion of said liner, wherein said first impurities are positioned within the portion of said liner adjacent said first conductive layer and second impurities are positioned within the portion of said liner adjacent said second conductive layer.

30. (Currently Amended) ~~The integrated circuit chip in claim 29,~~ An integrated circuit chip comprising:
a first conductive layer;
a liner on said first conductive layer, said liner including a barrier, said barrier impeding first impurities from diffusing from said first conductive layer through said liner; and
a second conductive layer over said liner, wherein said barrier impedes second impurities from diffusing from said second conductive layer through said liner,
wherein said barrier is limited to a central portion of said liner, wherein said first

impurities are positioned within the portion of said liner adjacent said first conductive layer and second impurities are positioned within the portion of said liner adjacent said second conductive layer, and

wherein said barrier comprises a concentration of a passivating agent less than an amount necessary to form a stoichiometric combination with said liner.

31. (Previously Presented) The integrated circuit chip in claim 30, wherein:
said liner comprises one of tungsten, titanum, molybdenum and nickel;
said passivating agent comprises one or more of nitrogen and chlorine; and
said second conductive layer comprises one of tungsten and copper.

32. (Currently Amended) The integrated circuit chip in claim ~~29~~ 30, wherein said impurities comprise one or more of silicon impurities and fluorine impurities.